

Single Event Upset and Latchup Measurements in Avionics Devices Using the WNR Neutron Beam and a New Neutron-Induced Latchup Model

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Abstract

Microelectronic devices used in avionics were tested in the WNR beam, simulating atmospheric neutrons. The SEU upset rates for ARINC 429 receivers agree with rates in memories, and neutron-induced latchup was measured in the LCA100K and 200K gate arrays and compared against a new neutron-induced latchup model.

INTRODUCTION

Devices of interest to avionics designers may be susceptible to single event effects induced by the atmospheric neutrons [1]. This has been demonstrated for upset (SEU) by upsets recorded in memories during flight [1], and also by upsets caused by the neutron beam at the Weapons Neutron Research (WNR) facility in two types of devices, memories [2,3] and microcontrollers [2]. The WNR beam at Los Alamos very accurately simulates the effects of atmospheric neutrons since it has the same energy spectrum as neutrons in the atmosphere, but is $\sim 3E5$ times more intense [2]. For latchup (SEL) this has been demonstrated in one type of device, large scale gate arrays using the WNR beam [4].

We report here on new measurements of both SEU and SEL with the WNR beam. In the case of SEU, the upsets were measured in three versions of a unique avionics device, the ARINC 429 receiver. In the case of SEL, large gate arrays from two different vendors were tested, two from one vendor experienced latchup and the single device from the other vendor did not. Heavy ion latchup data on one of the parts that latched up is available, and it will be used, in conjunction with a new neutron/proton-induced latchup model, to calculate the neutron-induced latchup rate that will be compared against the measured rate. In addition, the ARINC 429 receivers were also monitored for latchup, but none was observed.

ARINC 429 MEASUREMENTS AND RESULTS

Two each of three different ARINC 429 receivers were tested in the WNR beam. These are listed in Table 1. In all but one case, each device was tested at two different conditions: a) low or normal voltage and ambient temperature to enhance SEU and b) high voltage and 100 °C to enhance SEL. The three different devices were simultaneously exposed to the WNR beam, while being exercised. The test system sequentially transmits data to the devices and reads their contents. The registers tested are shown in Table 2.

Table 1 List of Devices Tested in WNR Beam

Device	Vendor	Description	SEE Effect Tested For
ARINC 429 Rcvr	US2, 3.3V	CMOS, 0.7 μ m, 5 μ m epi layer	SEU, SEL
ARINC 429 Rcvr	US2, 5.0V	Bulk CMOS, 1.25 μ m	SEU, SEL
ARINC 429 Rcvr	AMI, 5.0V	Bulk CMOS, 1.0 μ m	SEU, SEL
Gate array	Fujitsu, CGD3302	77K gates, 9K RAM bits	SEL
Gate array	LSI Logic LCA100K	Bulk CMOS, 1.0 μ m, 1E5 gates	SEL
Gate array	LSI Logic LCA200K	Bulk CMOS, 0.7 μ m, 2E5 gates	SEL

Table 2 ARINC 429 Receiver Registers Tested

Register	No. bits tested
Command reg A	4
Command reg B	5
Input reg	32
FIFO stack	256 (8x32)
VOE bit	1
Word Counter	4
Label Pointer	4
Label memory	128 (16x8)
Total	434

During exposure, the ARINC devices were continuously exercised using a test aid specifically designed for testing three devices in parallel. The test system firmware performed an upset detection loop, in which a variety of bit patterns were loaded into the receivers, read, and checked. The test loop was repeated at approximately 100ms intervals. Detected upsets were sent to data recording instrumentation via RS-232 interface. Test system control and data recording was accomplished through the use of a portable Macintosh computer running terminal emulation software.

To perform latchup testing, the supply currents drawn by each test device was monitored. A current spike three times the normal level indicated latchup. If latchup were to occur,

power was to be immediately shut off for approximately 20 ms and subsequently restored. Such latchup events were then to be counted using high-speed NIM scalars. Additional circuitry was employed which allowed the test system to temporarily shut off device under test (DUT) power should loss of functionality occur. However, as indicated, none of the parts latched up.

As shown in Table 2, a total of 434 bits were monitored for upset, mostly word bits (256) and label bits (128), along with a few register bits. A total of 29 upsets were recorded, 21 in the word bits and 8 in the label bits. The word/label upset ratio of ~2.6 is close to the ideal ratio of 2 that would be expected based on the number of bits being monitored. Results of the testing are tabulated in Table 3. We note that the AMI devices showed no upset, but both US2 types did.

COMPARISON OF ARINC 429 RESULTS WITH AVIONICS SEU RATES

Table 3 contains details and results of the tests. To make the raw upset data meaningful, we calculated the atmospheric error rate that would apply at 40,000 ft, based on: a) the neutron fluence experienced by each device, b) the hourly neutron flux at 40,000 ft (5800 n/cm²hr, E>10 MeV) and c) the number of bits monitored for upset. These bit error rates are listed in the last column of the table. Combining the results for all four runs for each part, we obtain the average bit error rates for the US2 parts as 7.3 E-10 upset/bit-hr for the 3.3 V part and 6E-10 upset/bit-hr for the 5V part. These bit upset rates fall in the same range as the upset rates in SRAMs that have been observed in-actual flight (~3-16 E-10 upset/bit-hr at altitudes of 29-35,000 ft [1]). These in-flight rates are based on data from three different SRAMs and can be converted to the following rates at the same 40,000 ft altitude, ~5-35 E-10 upset/bit-hr. Therefore, on a per bit basis, memory bits in standard SRAMs and in the US2 ASICS, exhibit similar sensitivity to neutron-induced single event upset.

Table 3. ARINC 429 WNR Test Data

Test Device	Serial No	Temp. (°C)	Supply Voltage (volts)	Word Upsets	Label Upsets	Neutron Fluence (cm ⁻²) [†]	Bit Error Rate [upsets/bit-hr (@40 kft)]
US2, 3.3V	10	ambient	3.3	4	0	5.1E+10	1.0E-9
US2, 3.3V	10	100	3.3	4	2	1.4E+11	5E-10
US2, 3.3V	6	100	3.4	3	3	7.5E+10	1.1E-9
US2, 3.3V	6	ambient	3.2	0	0	2.5E+10	<5E-10
US2, 5.0V	40	ambient	5.0	2	0	5.1E+10	5.2E-10
US2, 5.0V	40	100	5.25	2	2	1.4E+11	3.8E-10
US2, 5.0V	3	100	5.25	4	1	7.5E+10	9E-10
US2, 5.0V	3	ambient	4.75	2	0	2.5E+10	1.1E-9
AMI, 5.0V	50	ambient	5.0	0	0	5.1E+10	<3E-10
AMI, 5.0V	50	100	5.25	0	0	1.4E+11	<1E-10
AMI, 5.0V	51	100	5.25	0	0	7.5E+10	<2E-10
AMI, 5.0V	51	ambient	4.75	0	0	2.5E+10	<5E-10

[†] The WNR facility neutron beam intensity was approximately 4E5 n/cm²/s. Thus, most test runs lasted for several days, with only brief periods of beam "down time".

LATCHUP MEASUREMENTS AND RESULTS

Large scale gate arrays from two different vendors were obtained for the latchup only test. The devices tested are listed in Table 1. LSI Logic 100K and 200K devices had been tested previously in the WNR beam and were observed to latchup [4]. For this test an LSI Logic gate array, the 200K device, was obtained that had been previously tested for latchup with heavy ions [5]. A plot of the latchup cross section as a function of LET is shown in Figure 1. In addition, a 100K LSI Logic device was also tested, but no heavy ion latchup data are available on it.

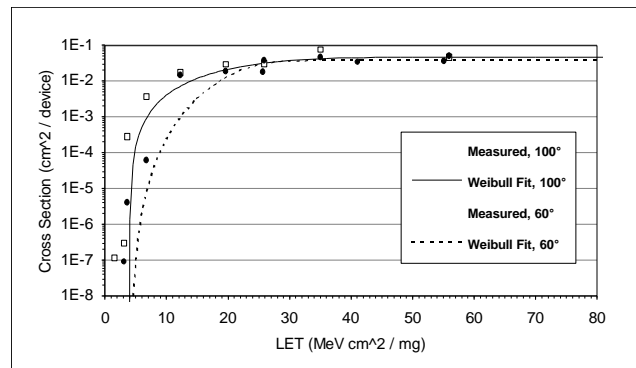


Figure 1 Heavy Ion Latchup Cross Section in LSI Logic LCA200K Gate Array

As far as is known, the Fujitsu gate array had never before been tested for latchup with either heavy ions, protons or neutrons.

The latchup results from this 1994 test are generally consistent with the previous 1992 results [4], as shown in Table 4. There were a number of changes between this and

the previous test, e.g. differences in beam line, exposure and parts monitoring conditions, etc., and we were not able to obtain as good statistics as in the earlier test. Only one latchup was experienced in each of the LSI Logic devices and none was observed in the Fujitsu gate arrays. Table 4 compares these results.

Table 4. Comparison of Latchup Testing of Gate Arrays in WNR Beam

Part	Test Year	Equiv Flight Hours @ 4E4 Ft	WNR fluence > 10 MeV, n/cm ²	Number Latchup	Latchup/ Flight Hr
LCA100K	1994	5.56E+6	3E+10	1	1.8E-7
LCA100K	1992	2.46E+7	1.3E+11	19	7.9E-7
LCA200K	1994	2.6E+7	1.4E+11	1	3.9E-8
LCA200K	1992	5.6E+6	3E+11	7	1.2E-7

DISCUSSION OF LATCHUP RESULTS

Having the heavy ion latchup cross section for the LCA200K should allow us to estimate the neutron-induced latchup rate for this part if an appropriate latchup model were available. A measure of the accuracy of the model could be made by comparing the calculated neutron-induced latchup rate against the data in Table 4.

For upset, a number of simple models [1], each based only on energy deposition, have been shown to adequately calculate the neutron/proton SEU rate [1]. We prefer the burst generation rate (BGR) method for carrying out these calculations for neutron/proton-induced upset [1]. The BGR method does not require the use of existing proton SEU data which often isn't available, but it does require that heavy ion cross section data be available, and it has generally been based on BGR functions calculated for an infinite medium of silicon.

Preliminary calculations with the BGR method, based solely on energy deposition, unfortunately showed that this method was far too conservative when applied to latchup. For what might be considered reasonable collection thicknesses of ~4-8 μm, the calculated latchup rate for the LCA200K device, using the latchup data in Figure 1 was, between 30-200 times higher than the results in Table 4. The need to develop more complex models to explain proton/neutron-induced latchup has previously been recognized [6]. One such model, based on the track electric field reduction of the LET of the neutron-induced recoils, has already been developed [6]. While this model appears to give good results when compared to measured proton-induced latchup cross sections [6], the tools needed to implement it are not readily available.

Thus we chose to develop our own new latchup model that has the following key elements: a) it incorporates geometric factors that are based on standard microelectronics design practices, as well as on some preliminary specialized heavy

ion latchup test results, b) it uses the general BGR methodology but for smaller sensitive volumes, and c) it uses heavy ion latchup cross section data.

NEW PROTON-INDUCED LATCHUP MODEL

We initially conjectured that the energy deposition needed to turn on and sustain the latchup mechanism was dependent on not only the LET of the ion depositing the energy but also the range of the ion. To demonstrate this we designed a simple test based on use of an actual part that was known to be very susceptible to latchup, the CY7C261 EPROM. The part was tested with a number of different ions with different LETs and latched up; the device latchup cross section as a function of LET is shown in Figure 2. We then covered the delidded part with several different thicknesses of laboratory grade aluminum foil, the purpose being to reduce the range of the ion, while not changing its LET by very much. Figure 3 shows the theoretical calculations using the TRIM code [7] for how the range and LET of the Co ion in silicon vary with different thicknesses of aluminum shielding. Curves for Kr and Ar ions show the same type of behavior.

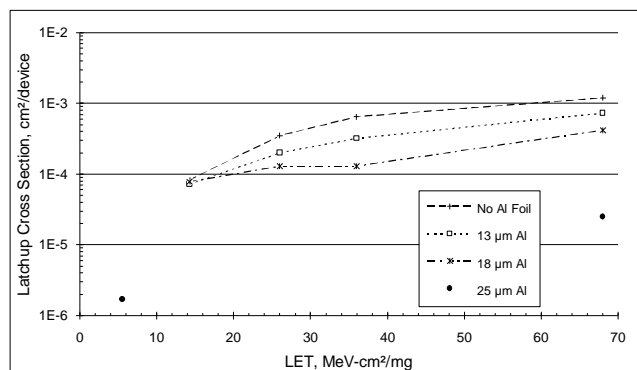


Figure 2 Single Event Latchup Heavy Ion Cross Section (cm²/device) in CY7C261 As Function of LET and Aluminum Foil Thickness Reducing Effective Range of the Ion

Figure 2 shows that as the foil thickness increased, the latchup cross section decreased, and then finally disappeared when the shielding was 25 μm . From Figure 3 we see that the Co ion started out with an LET of 26 $\text{MeV cm}^2/\text{mg}$ and a range of 38 μm in silicon. After going through 25 μm of aluminum the LET of the resulting ion is initially 30 $\text{MeV cm}^2/\text{mg}$ with a range of 10 μm . Its LET is large enough to cause latchup, but its range is not and so no latchups result. We assume that the glassivation/passivation layers over the silicon are thin, typically 1-3 μm in thickness. Thus, we conclude from this simple experiment that to sustain latchup, there is a minimum range that ions even with high LETs must possess, and it is approximately 10 μm for this part. Since we have not accounted for the over burden (passivation layers), the minimum range is estimated to be 6-10 μm .

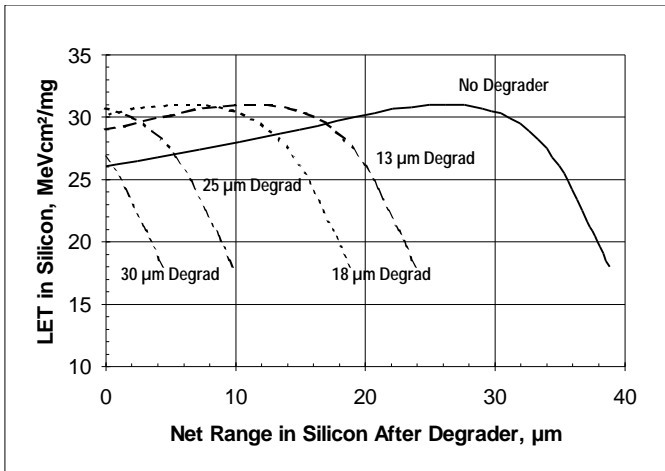


Figure 3 Variation of LET and Range of the Co Ion (4.5 MeV/amu) in Silicon As Function of the Thickness of Aluminum Degradation

If a minimal range is required of heavy ions to initiate latchup, it is also required of the recoils created by neutrons and protons interacting with silicon. Thus, one part of the neutron-induced latchup model requires that the range of the recoils that contribute to latchup must be $> 6-10 \mu\text{m}$. Most of the lower energy recoils have ranges considerably less than this. By imposing this range requirement that was derived from latchup experiments, we obtain a limitation on the contribution of the LET or energy deposition of the recoils, and this has a similar effect as the track electric field reduction of the LET of the recoils used in the previous model [6].

The next part of the model assumes that latchup occurs at fixed sites on a device where the required parasitic transistors are located close enough to one another that ions with a range of 6-10 μm and a high enough LET can deposit enough energy to turn them on. The geometry is shown in Figure 4 in terms of the n+ transistors within the p-well and the lateral and vertical transistors that get turned on. The calculation for energy deposition for latchup has to be based on a relatively small volume that in reality is L-shaped

(combination of lateral and vertical transistors in Fig. 4), but which we idealize as a rectangular parallelepiped approximately $8 \mu\text{m} \times 8 \mu\text{m} \times 5 \mu\text{m}$ (deep). More generally, the lateral transistor width, which may be called the characteristic length or sensitive width [11], varies from device to device, but is generally in the range of 4-10 μm , although it may be as wide as the entire p-well in some cases. The p-well breadth, i.e., the transverse dimension, is longer; it can be 50 μm or larger. In actual devices, p-well areas on a single chip are often of different sizes and shapes.

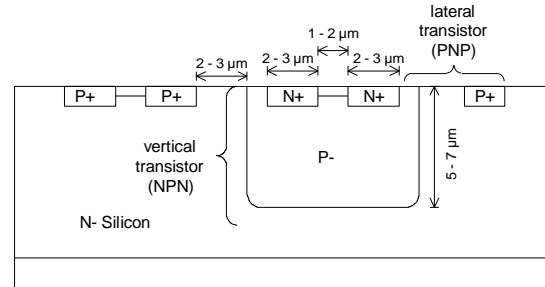


Figure 4 Geometric Representation of CMOS Structure with Parasitic Transistors

Thus accounting for the true geometry of an actual device may be difficult unless complete part layout information is available from the microelectronics vendor, which is almost never the case. Our model is therefore viewed as a simplified first step in accounting for proton-induced latchup that considers the key geometrical and energy deposition factors. It is implemented by dividing the device heavy ion latchup cross section by the area of the transistors ($8 \mu\text{m} \times 8 \mu\text{m}$ in this example) to find the total number of such latchup sites. The energy deposition by neutron-induced recoils that leads to latchup is calculated for a single sensitive volume, and then multiplied by the total number of latchup sites.

To calculate how much energy is deposited into the sensitive volume in order to induce latchup, the BGR method is used. BGR functions are calculated based on only neutron/proton interactions in the silicon, to quantify the probability that a neutron/proton of energy E_p will produce recoils of greater than energy E_r , $BGR(E_p, E_r)$ [1,8]. However, almost all of the published BGR values are based on an infinite medium of silicon. For a smaller volume of silicon, the total number of interactions taking place will be the same, but there will be many more lower energy recoils and many fewer higher energy recoils compared to the infinite medium case. Several years ago calculations were carried out with the LAHET computer code [9] to determine BGR functions for two smaller volumes in addition to the infinite medium, but these were never published [10]. One of these small volumes, $10 \mu\text{m} \times 10 \mu\text{m} \times 2.5 \mu\text{m}$, is close to the sensitive volume that we have described above as pertaining to the latchup phenomenon. We have used these initial BGR functions for the small volume as applying to the

latchup site (lateral and vertical transistors), and then reduced them based on the recoils having a minimum range (6-8 μm), in order to obtain the appropriate BGR functions for initiating

latchup as described above. These resulting reduced BGR functions for the $10 \times 10 \times 2.5 \mu\text{m}^3$ volume are shown in Figure 5.

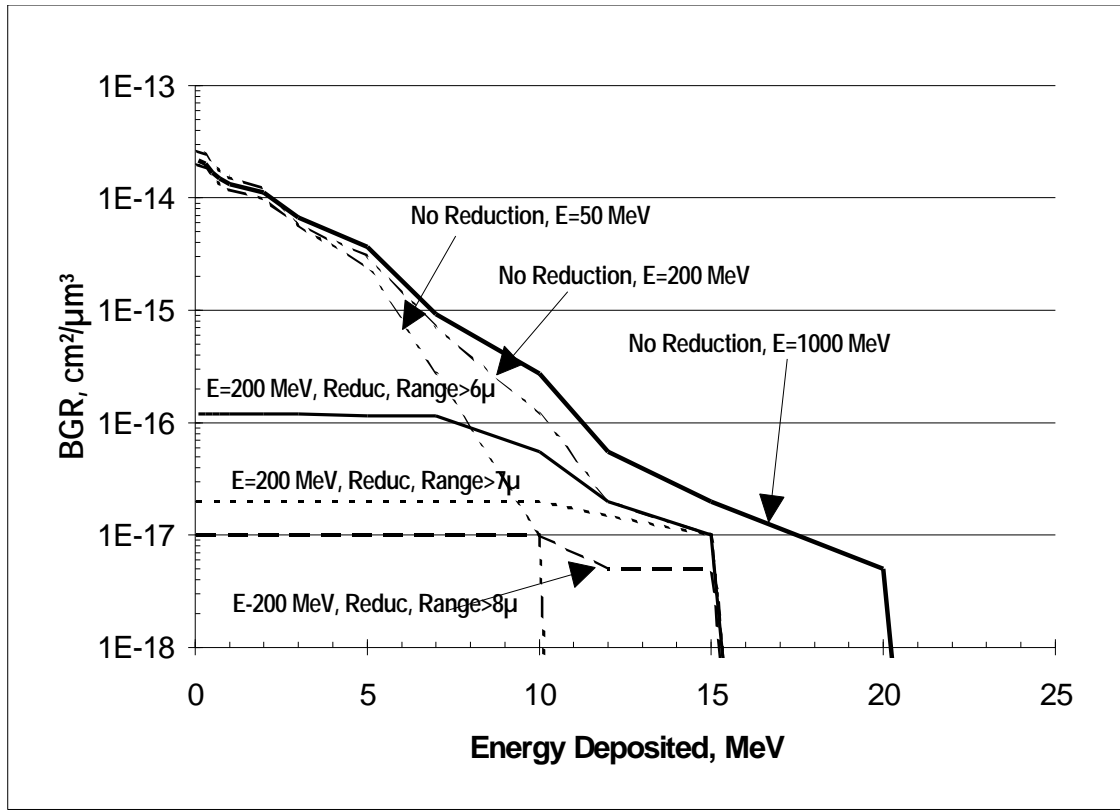


Figure 5 Burst Generation Rate Function, $BGR(E_p, E_r)$ for Energy Deposition by Energetic Protons/Neutrons in $10 \times 10 \times 2.5$ Volume of Silicon

CALCULATED RATES WITH NEW NEUTRON-INDUCED LATCHUP MODEL

The resulting latchup rate in the WNR beam was calculated using the aforementioned BGR functions using the formulation [1]

$$\text{Upset Rate} = C \sum_i \Delta V_i \int_E BGR(E, E_{ri}) (dN / dE) dE \quad (1)$$

Where t = sensitive thickness, (collection depth for latchup) μm

$\Delta \sigma_i$ = heavy ion SEU cross section for i th portion of curve, cm^2

= $\sigma_i - \sigma_{i-1}$ (obtained using the Weibull fit)

ΔV_i = $t \Delta \sigma_i$, μm^3 = sensitive volume

LET_i = representative LET for i th portion of curve, $\text{MeV cm}^2/\text{mg}$

E_{ri} = $t \times 0.23 \times LET_i$, MeV

BGR = burst generation rate, $\text{cm}^2/\mu\text{m}^3$, probability that particle of energy E will produce recoils of energy $\geq E_{ri}$

C = collection efficiency

The results, which are shown in Table 5, indicate that this preliminary version of the new neutron-induced latchup model is capable of predicting, within less than an order of magnitude, the latchup rate induced by the WNR neutron beam, i.e., the latchup rates found in Table 4. In carrying out the calculations using Eq.(1), a number of assumptions were required. The reduced BGR functions for $E_n=200$ MeV were used and applied to the atmospheric neutrons at 40,000 ft for $E>100$ MeV (a flux of 2900 $\text{n}/\text{cm}^2\text{hr}$, or half of the $E>10$ MeV flux of 5800 $\text{n}/\text{cm}^2\text{hr}$). The Weibull fit for the LCA200K gate array at 100 °C shown in Fig. 1 was used, along with the assumed $10 \times 10 \mu\text{m}^2$ latchup site area (resulting in 47,000 latchup sites/device) and C was taken to be 1.

The model provides good agreement with the measured rates by requiring the neutron-induced recoils to have a range in silicon of 6-8 μm , the same range in silicon which was obtained in the special latchup test results pictured in Figure 2. For protons/neutrons of 200 MeV, the model can be applied to other devices prone to proton-induced latchup by utilizing the reduced BGR functions in Fig. 5, along with a functional fit to the SEL cross section as a function of LET.

Table 5 Comparison of Measured Latchup Rates in LCA200K with Those Calculated Using New Neutron-Induced Latchup Model

	Calculated with New BGR-Based Latchup Model Latchup/Hr at 40,000 Feet Altitude		
Measured Rate, Latchup/Flight Hr	Range Reduction =6μm	Range Reduction =7μm	Range Reduction =8μm
3.9E-8 (1994)	2.2E-7	9.0E-8	2.6E-8
1.2E-7 (1992)			

CONCLUSIONS

Microelectronic devices used in avionics applications have been tested in the WNR beam, simulating the effect of atmospheric neutrons in inducing single event upset and latchup. The SEU upset rates on a per bit basis for the ARINC 429 receivers are in good agreement with the upset rates that memories have experienced in flight. Neutron-induced latchup in the LCA200K gate array is similar to previous results, but was performed on a part having heavy ion latchup cross section data. A preliminary version of a new model for neutron-induced latchup was introduced and the latchup rate it calculated was in good agreement with the measured rates.

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